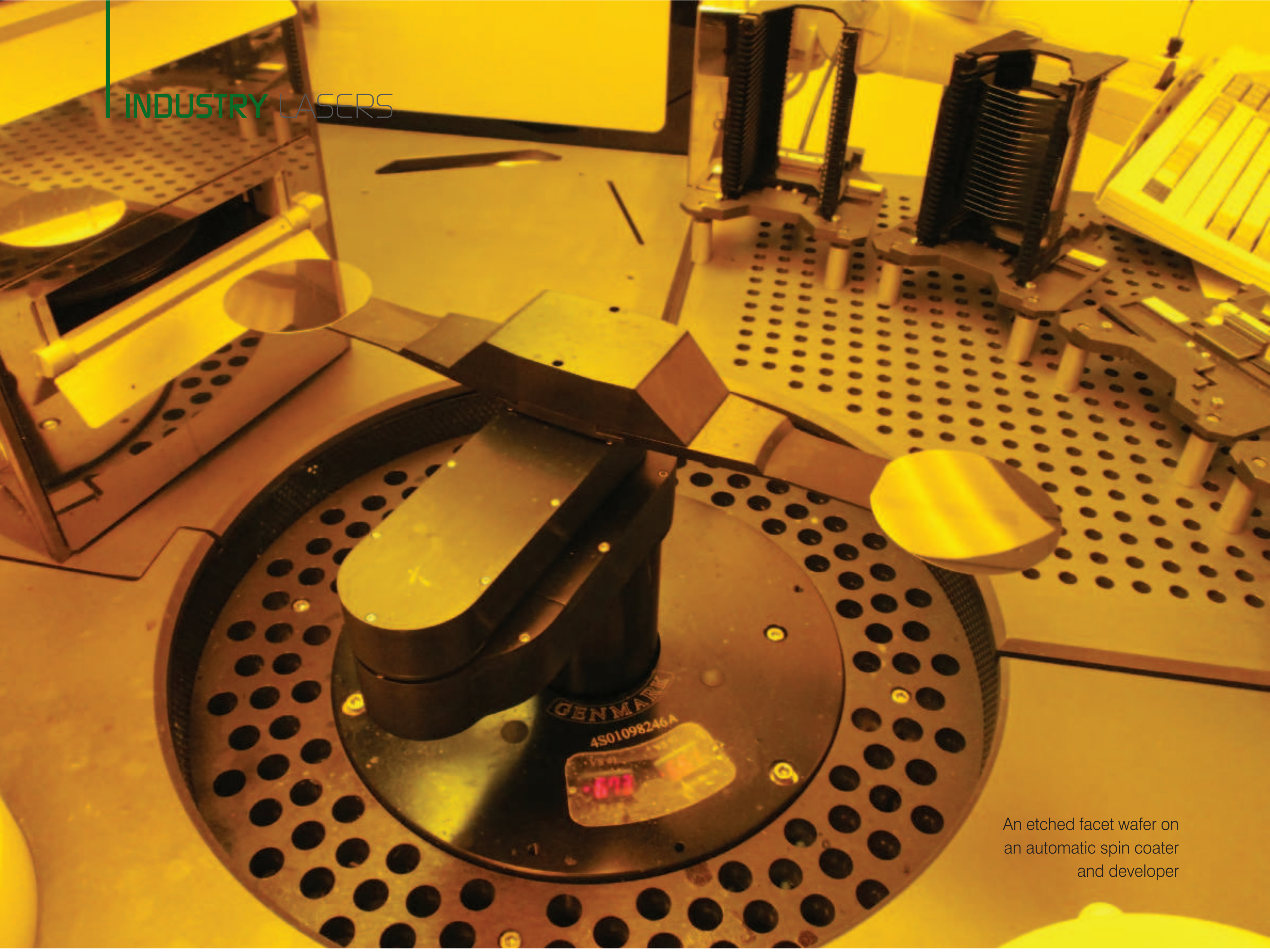


An etched facet wafer on an automatic spin coater and developer

Lighting up silicon photonics

The etched facet laser is an attractive candidate for silicon photonics, thanks to its small dimensions, freedom from hermetic sealing and its compatibility with passive alignment to waveguides

By ALEX BEHFAR FROM BINOPTICS

SURGING SALES of smartphones, increased video conferencing and the growth on Internet TV are placing increasing demand on computing power and the providers of data communications. To alleviate the strain, many industry experts are expecting that integrated circuits will soon get a new lease of life through the introduction of photonic links, which will predominantly come in the form of chip-to-chip and on-chip photonics.

These optical technologies will make a tremendous impact on the future of computing. Although this market is in its infancy, revenues for the silicon photonics industry are rising fast and should exceed $2 billion by 2015, according to Market&Markets.

Already active in this area are several of the leading names in the computing and communications industry. IBM, Cisco, Oracle, Mellanox and Luxtera are all publicly discussing their work on silicon photonics and their plans for its use in the future, while Intel and others are already turning to silicon photonics for data networking, in an effort to dramatically boost efficiency in data centers. Deployment of this technology is underpinned by the efforts of researchers, who are devising ways to slash the cost of large-scale silicon photonics development.

A key component in any photonic circuit is the light source. This tends to be an InP laser, because its spectral range is transparent to silicon. Today, three formats of this device are being used for this application: the cleaved facet laser, the hybrid silicon laser and the etched facet laser.

By far the most mature of these three is that based on a cleaved facet – chipmakers have manufactured hundreds of millions of them. As its name suggests, this type of laser is produced by cleaving an epiwafer to form an atomically flat surface. During the production process, engineers make edge-emitting lasers by cleaving wafers into bars, applying mirror coatings to the facets and then separating the bars into discrete chips. These are often hermetically sealed to ensure reliable operation.

One company that has fabricated a cleaved facet laser in a hermetic enclosure for use with silicon photonics chips is Luxtera. Its package, which also features a ball lens and a reflector, provides a reliable source of light that can be coupled into the silicon photonics chip.

An alternative light source, the hybrid silicon laser, is formed using a glass glue to fuse an InP gain chip to silicon. This relatively new approach, which has been championed by Intel for silicon photonics applications, uses the InP-based structure for light generation and amplification, with the laser cavity formed via the hybrid integration of the InP-based structure to the silicon-based waveguide.

The third approach – etched facet technology – has been pioneered by our team at BinOptics of Ithaca, NY. Its merits include the definition of facets through high-precision photolithography, rather than imprecise, hit-or-miss, mechanical cleaving. This ensures unprecedented uniformity and yield, as well as the capability to build structures that cannot be made with conventional techniques. Since our founding in 2000, we have fabricated over 50 million etched-facet lasers with this technology.

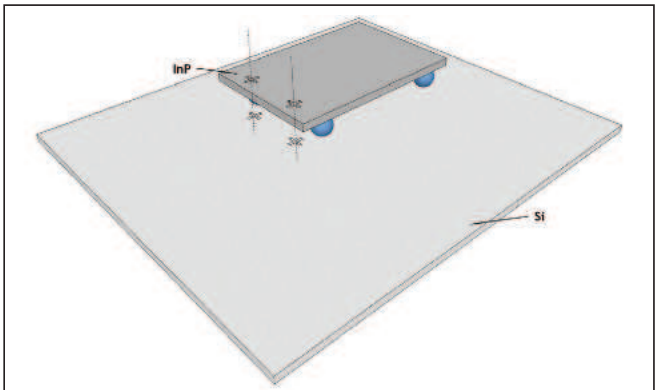


Figure 1. BinOptics facet-etching technology enables passive alignment of the laser to the waveguide. This is possible because the location of the InP chip relative to an alignment mark or a fuducial can be known to within 0.1 μm

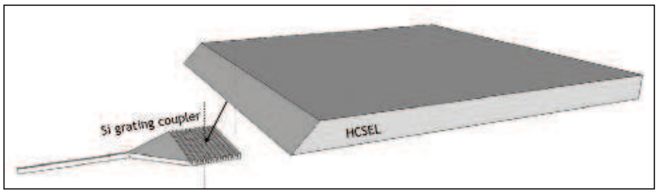


Figure 2. BinOptics' horizontal cavity surface emitting laser (HCSEL) features an etched facet at an angle off from 45°. This ensures that the laser beam emerges at an angle to the gratings on the silicon photonics chip. The HCSEL has its electrical contacts on its surface and is flip-chip mounted onto the silicon photonics chip.

Ticking the boxes

For wide-scale adoption in silicon photonics, there are three key requirements for the light source: it must be available as known good die; it has to survive without a hermetic package; and it must be able to be passively aligned to the silicon photonics chip, rather than requiring active alignment.

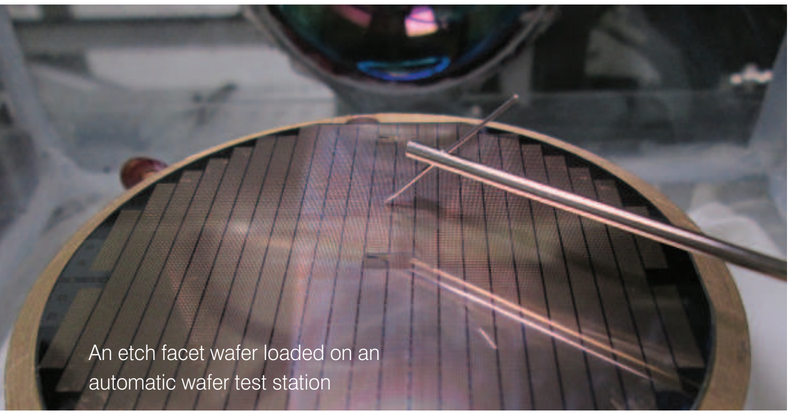
To meet the known good die criteria, the laser must deliver a high level of performance, even at temperature extremes. Device performance is evaluated by measuring light-current-voltage characteristics and spectral profiles at various temperatures. Benchmarking may include a certain threshold current for the laser to start lasing; a minimum light output at a certain current; and a side-mode-suppression-ratio – extracted from the spectral measurements – that exceeds a minimum value.

One of the weaknesses of a silicon hybrid laser is that the InP chip cannot be assessed for whether it conforms to known-good-die criteria until after it has been integrated with the silicon platform. If a bad chip is to blame for a faulty final package, it is costly, if not impossible, to replace this sub-standard gain chip.

Applying a hermetic seal is a common approach to increasing the reliability of an InP laser. But this is not an option for the entire silicon photonics circuit, due to cost and size requirements. To reap the size benefits that silicon photonics offer, the InP laser must be flip-chip mounted to the silicon photonics chip or wafer. And if the InP chip normally requires a hermetic package, this has to be applied to the integrated package of the InP chip and silicon photonics chip — and that would create a component that would be too expensive and bulky for most applications of silicon photonics. So, given all this, it is easy to see why InP light sources that do not require a hermetic package are very attractive for InP photonic applications.

Hermetic sealing is widely used with cleaved facet edge-emitting lasers, which typically feature a waveguide between the front and back facet to ensure the guiding of the light within the semiconductor. Deposition of dielectrics aids waveguiding and can tune the reflectivity of the facets, leading, for example, to a highly reflective back facet and a low reflectivity front facet.

Degradation can occur in this class of laser if it is housed in a non-hermetic environment. If there is a discontinuity between the dielectrics on the facets and the waveguide then, over time, moisture will penetrate through this discontinuity and compromise the quality of the semiconductor. And if the dielectric is permeable to moisture, this will be absorbed,



An etch facet wafer loaded on an automatic wafer test station

leading to increases in the dielectric volume and stress in the dielectric. Slow separation of the dielectric from the facet then occurs to expose the semiconductor, which degrades in this environment.

What's more, most cleaved facet lasers are impaired by a discontinuity between the waveguide dielectric and the dielectrics on the facets. So, to avoid degradation, a hermetic package is added. It is worth noting that the dielectrics, which are deposited with an electron-beam evaporator, do offer some protection from the external environment for the facets that they coat. However, in general, their quality is insufficient to provide protection for any extended period of time in a non-hermetic environment.

In comparison, with our lasers that have facets formed by etching rather than cleaving, it is possible to provide continuous coverage of the waveguide surface and the facets with a dielectric. This coating may be applied by plasma-enhanced CVD, which can produce high quality films that are impermeable to moisture. Thanks to this, etched facet lasers do not require a hermetic package. This claim is supported by our study, which revealed that etched facet lasers can successfully operate in 85 percent relative humidity and 85°C for at least 5000 hours, without the need for a hermetic package.

One opportunity for significant cost reductions associated with the fabrication of photonic circuits is to switch from active alignment to passive alignment – it can be up to ten times cheaper. With active alignment, the laser is powered up and moved around until sufficient light is coupled into the silicon photonics waveguide. Once that is achieved, this emitter must

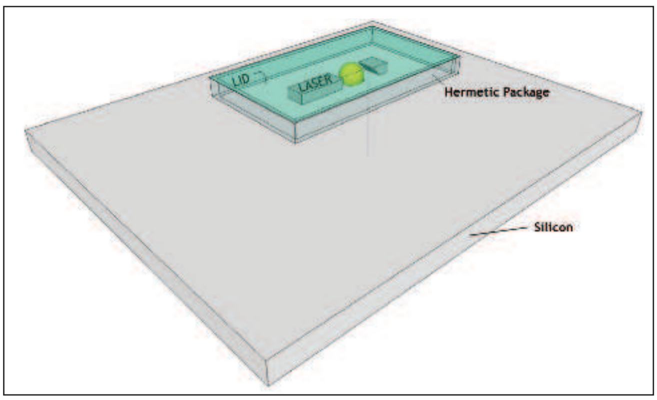


Figure 3. A cleaved fact laser can couple light into a narrow waveguide via a grating coupler

be locked down in place on the silicon photonics chip, as any additional movement would reduce the proportion of light coupled into the silicon photonics waveguide. Doing this is a slow, costly process that is not acceptable for many silicon photonics applications.

Although turning to passive alignment slashes costs, even under the best circumstances the facets of a cleaved facet InP-based laser can only be positioned to within $\pm 2 \mu m$ of the desired location. Depending on the dimensions of the waveguide – which are discussed shortly – this may not be good enough.

With our InP-based laser that has facets formed by etching, this situation is markedly different. In this case the facets are lithographically defined, so it is possible to know their location relative to an alignment mark or a fuducial to within 0.1 μm, which is more than sufficient (see Figure 1).

Note that with a hybrid silicon laser, there are no alignment issues, because the glass glue process removes the need to align the InP gain wafer to the silicon photonics wafer.

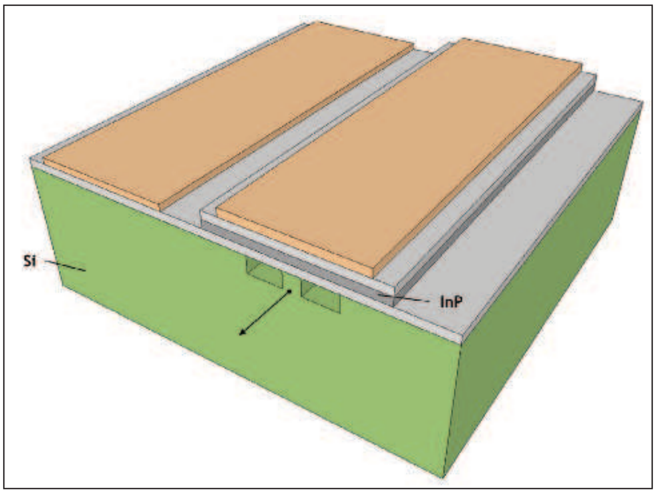


Figure 4. Hybrid silicon lasers offer alignment-free coupling of a laser into a silicon wavguide

Waveguide dimensions

Silicon waveguides have a range of dimensions, and this has a big impact on how difficult it is to couple light into them. In general, there are two types of silicon photonics waveguides: large ones with dimensions of around 3 μm, which are used by Mellanox (formerly Kotura); and those that are 400 nm or narrower, used by IBM and others.

Large waveguides are well matched to the mode size of a typical InP-based laser. Thanks to this, it is relatively easy to realise efficient, direct coupling of the laser into these large silicon photonics waveguides. Edge-emitting lasers, as opposed to their surface-emitting cousins, are well suited to coupling light into these types of waveguides. Shrink the dimensions of the waveguide, however, and the situation changes dramatically. In this regime, some form of mode convertor is often employed to aid the coupling of laser light into the silicon photonics waveguide. One option is to use an adiabatic taper. Ideally, the light from the laser has a narrow beam divergence and impinges on the grating with an incidence angle that is off from perpendicular. If this angle is optimal, any back-reflection from the grating to the laser is eliminated.

With our InP-based, horizontal-cavity surface-emitting laser that features etched facets at an angle off from 45°, the laser beam emerges at an angle to the gratings on the silicon photonics chip (see Figure 2). Light is then directed to the narrow silicon photonics waveguide through the gratings and an adiabatic taper.

A cleaved facet laser, packaged with a ball lens and a reflector in a hermetic enclosure, is also capable of directing the laser emission at the right angle to ensure a high intensity of light in the narrow waveguide (see Figure 3). If this cleaved-facet laser package is mounted to the silicon photonics chip, a hermetic package is not required around the combined chip. Although this means that additional optical elements beyond the laser are required, on the plus side only a relatively small hermetic package is needed around the cleaved facet laser.

It is not yet clear whether a hermetic package is needed for a hybrid silicon laser that is employed to couple light into a narrow waveguide on the silicon photonics chip (see Figure 4). If it's not needed, this approach that Intel introduced is attractive, given that it is also alignment-free when the InP wafers are bonded to the silicon wafer.

Another issue to consider is the significant difference in the dimensions of the different InP lasers being considered for silicon photonics. Cleaved and etched facet laser chips are relatively small, with typical lengths and widths of around 300 μm and 250 μm, respectively. This means that they use up just 0.075 mm^2 of InP real estate, which is several orders of magnitude less than that of the hybrid laser – it is expected to have similar dimensions to the silicon photonics chip, such as 5 mm by 6 mm. However, this issue may be alleviated with an InP die attach process that involves using glass glue to bond the InP gain chips, rather than the full InP wafer, to the silicon photonics wafer.

Our survey of the three different light sources for silicon photonics – cleaved lasers, hybrid lasers, and etched fact lasers – shows that they all have some pros and cons. The ideal approach will ultimately depend on the desired final function, and how these technologies progress as silicon photonics continues to gain popularity in the computing and datacom worlds. Whichever way you look at it, silicon photonics has a bright future, and it will be exciting to witness how this technology transforms the world as the digital age continues to unfold.

One of BinOptics' vacuum systems used in the production of etched facet lasers.

	Hybrid Silicon Laser	Etched Facet Laser	Cleaved Facet Laser
Attachment of InP to Silicon	Glass-glue fuses InP to silicon	Flip chip mounting	Flip chip mounting
Alignment	Alignment free	Passive alignment	Active alignment
InP Non-Hermetic Capability	Unknown	Yes	No
InP Known Good Die (KGD)	No laser is formed until integration of InP with Si	Yes; enabled by on-wafer testing over full temperature range	No; bar-level testing is usually only at room temperature
InP Laser	N/A	Yes	Yes
Maturity	New	50M+ devices shipped	100's of millions of devices shipped
Surface Emission	N/A	Yes	Yes, but requires external optical elements
InP Real Estate	Same size as silicon photonics chip if InP wafer bonding is used	300µm x 250µm	300µm x 250µm