HMIC Wafer Level Packaging

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***Abstract*- HMIC, an acronym for Heterolithic Microwave Integrated Circuits, is fundamentally a wafer level substrate which combines low, RF loss tangent glass with micromachined silicon to produce three dimensional circuitry with the capability to make RF, DC, and thermal vias as the device input and output. Using this technology both active and passive RF devices have been produced which have demonstrated excellent high frequency performance over a very broad range of frequencies from 1 MHz to as high as 110 GHz. This paper describes the development of a unique microwave and mmW packaging technique based upon the broadband high frequency properties of the basic HMIC technology. More specifically the results of utilizing the high frequency, 3-dimensional integration properties to provide a packaging medium that will enable active components, whether in flip chip or bondable configurations and including silicon, GaAs, or InP mixed materials, to be combined to create a surface mount wafer level multichip module is presented. It will be shown that this basic HMIC technology can also be applied to enable the incorporation of a hermetic solder seal silicon lid.**

I. INTRODUCTION

Historically, packaging for high frequency applications was limited to various ceramic metal configurations which generally were custom designed and fabricated for each specific die design and circuit function. While these ceramic packages performed quite well from HF through mmW frequencies, they have had and continue to have a very high cost and are generally not configured for surface mount procedures for higher level assembly. Due to .these limitations, the microwave industry moved to a stamped metal leadframes with various epoxy overmold compounds approach to realize the needed packaging. This approach has proved to be low cost and completely compatible with surface mount assembly, but has proved to have performance RF limitations at frequencies above a few gigahertz and in particular at mmW wavelengths.

Another direction that can be taken for high frequency packaging is based upon silicon which has low electrical resistance and a high thermal conductivity and glass which provides not only DC and RF isolation but also due to its very low loss tangent and a relatively low dielectric constant enables the incorporation of high Q passive elements and microwave transmission lines. This technology is designated HMIC, which is an acronym for Heterolithic Microwave Integrated Circuits referring to it's creation from two dissimilar materials. In this technology, two different materials, glass and silicon - thus, the term *hetero*, are joined into a single monolithic structure. From this marriage of glass and silicon, a synergism is obtained which enables the high frequency properties of the two materials to be optimized and obtain a wafer scale HF/microwave/mmW integration and packaging medium.

A generalized crossection of the HMIC structure is shown in Fig. 1. In this figure, it can be seen that the silicon vias, shown here as trapezoidal shaped pyramids, though vertical defined structures are also possible, extend through the entire thickness of the die and are completely surrounded by a sea of glass. The HMIC packaging concept takes advantage of the simplest function of these silicon pyramids is to provide a three dimensional electrical via to the DC and RF patterned back metallization for electrical input and output. Since the glass is totally transparent, a front to back alignment is trivial. Due to the high thermal conductivity of the basic silicon material, approximately one third that of gold, these vias may also be used to provide a low thermal path for high power

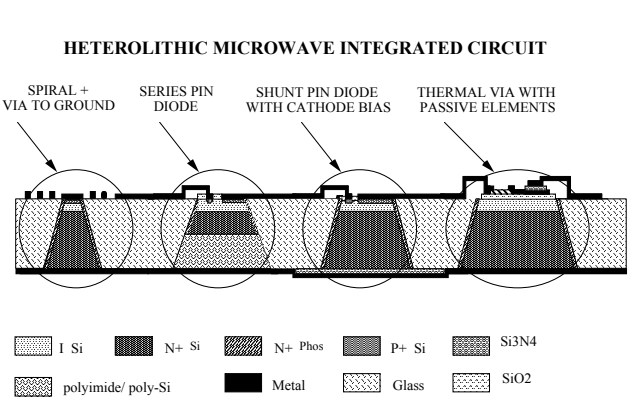

Fig. 1 Generalized Crossection of HMIC Structure

dissipative elements on the top surface to an underlying heat sink.

As high frequency packaging demonstrator an AlGaAs PIN diode SPDT switch which has frequency capability through 50 GHz, was chosen. While this AlGaAs PIN diode switch is normally produced as a chip and wire component, for this work a AuSn bumped version was developed and employed. This bumped configuration will enable the most aggressive packaging configuration in terms of size and multi-material

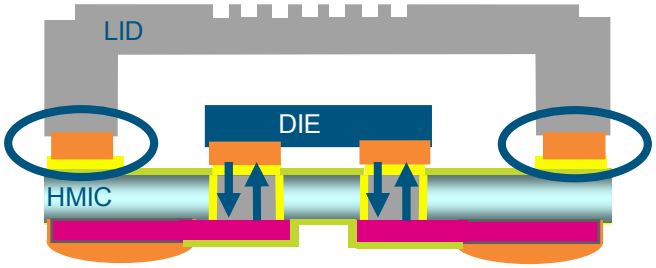

Fig. 2. Crossectional view of package concept. All I/O is vertical shown by arrows. No signal passes thru the continuous circled seal ring.

technology to be showcased. Fig. 2 is a crossectional view of this packaging concept. Also, a layout version of the AlGaAs SPDT switch with the translation to a AuSn bumped flip chip configuration is presented in Fig. 3.

Fig. 3 Shows the layouts of the HMIC substrate with the flip chip version of the SPDT. The elimination of wire bonds can reduce the size and improve the performance of the final packaged device.

II. HMIC Substrate Process

The first step in creating an HMIC based high frequency package is accomplished by micromachining a silicon wafer. This is accomplished either by a dry etch techniques or by a wet caustic etch. The etched areas of the wafer are then filled with an expansion matched low loss glass. See Fig. 4 and Fig. 5.

After etch the wafers are coated with a metal capable of process temperatures in excess of 700C such as cobalt silicide, titanium silicide, or silver. The expansion matched low loss glass is then applied, ground, and polished to the original silicon wafer surface as shown in Fig. 6.

Fig. 4. Crossection of etched silicon wafer.

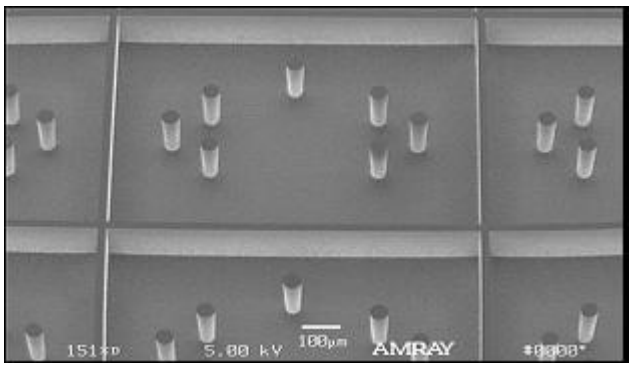

Fig. 5. SEM of HMIC substrate wafer after etch

Fig. 6 Crossection of HMIC substrate after glass processing

In essence the this construction is a via first process. The vias are metal wrapped around solid silicon which will eventually connect the two surfaces of a glass wafer. The HMIC substrate can be processed like a silicon wafer except temperature exposure should not exceed 600C.

Fig. 7 Crossection of HMIC substrate after metal deposition

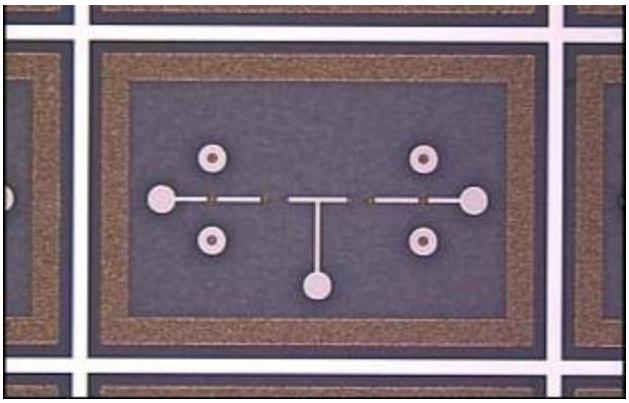

Fig. 8 Photomicrograph of HMIC substrate after metal deposition

The HMIC hermetic package process requires at least two layers of metal but can accommodate up to four layers of metal totaling 15 micrometers. The minimum two layers are shown. One layer of metal provides interconnect between multiple flip chip die attached to the substrate. The second

layer of metal is a stack of titanium platinum and gold/tin eutectic solder. See Fig. 7 and Fig. 8.

III. -HMIC Package – Active Device Integration

After the completion through AuSn metallization, of the HMIC substrate as described above, the next step is to populate the polished HMIC wafer with active components; in the present demonstration, the AuSn bumped SPDT AlGaAs die shown in Fig. 3 by flip chip die attach. In order

Fig. 9. Crossection of wafer after flip chip die attach

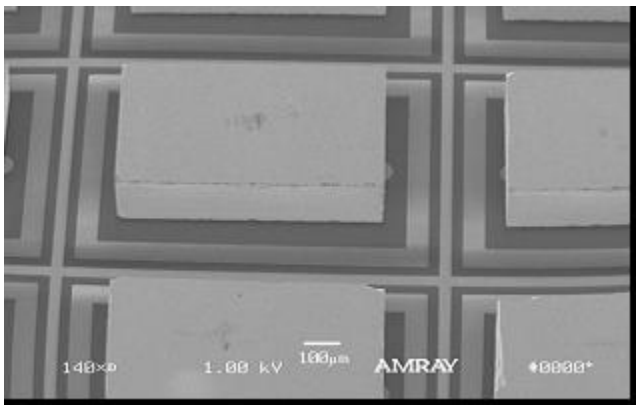

Fig. 10. SEM of HMIC wafer after flip chip die attach

to take advantage of the waferscale nature of the HMIC substrate, the flip chip die attach is accomplished by tacking the die in place using 5 to 10 microns of AuSn solder across the entire wafer using automatic, pattern recognition pick-and-place equipment followed by a reflow of the AuSn solder simultaneously attaching all of the die at the wafer level. A schematic crossection and SEM photomicrograph of this process is presented in Fig. 9 and Fig. 10.

After the wafer level die attach of the populated substrate is complete, the composite HIMC substrate is ready to be hermetically sealed by solder attaching a lid wafer. As can be

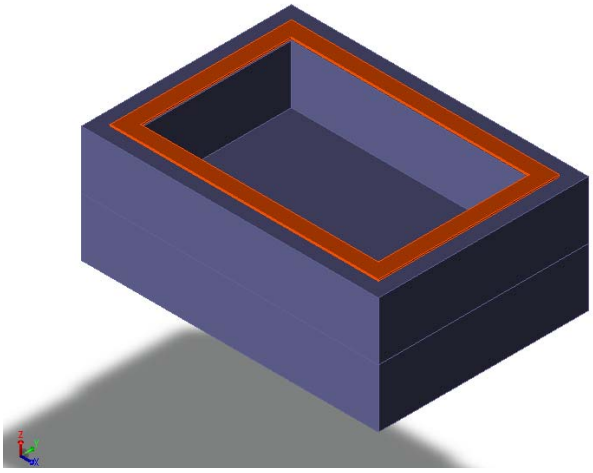

Fig. 11. HMLID1 Solder seal ring and etched cavity

seen in Fig. 11, the lid wafer is metalized with a mirror image of the seal ring pattern as the substrate. The lid wafer also has a cavity within the seal ring to accommodate the flip chip attached die; see Fig. 11.

The hermetic package enclosure of each die is accomplished by wafer bonding techniques. The wafer bonding is performed by aligning AuSn metalized lid wafer and the populated HMIC substrate wafer which are then

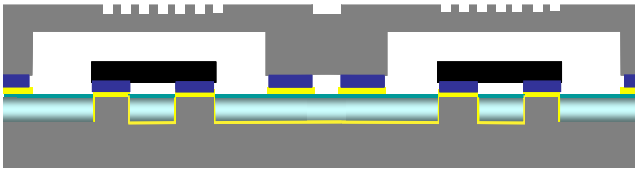

Fig. 12. Schematic crossection of HMIC package after lid seal

Fig. 13. Crossection of thin HMIC substrate to reveal vias

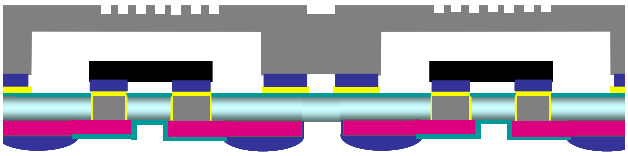

Fig. 14. Redistribution and solder bump metalization

moved to a bond chamber for solder reflow in a controlled environment. Wafer to wafer aligning and bonding is a well developed technology available commercially from several equipment manufacturers. One micron alignment is available but for this work 10 micron accuracy is sufficient. The sealing atmosphere is controlled in the bond chamber and can be vacuum, reducing, inert, or oxidizing. The HMIC package wafers of the present work were bonded in an inert atmosphere near 300C in a few minutes, as shown schematically in Fig. 12. Multiple bond chambers can be employed if higher throughput is desired.

The solder sealed HMIC package substrate is now ready to be thinned to reveal the electrical input and output vias and metalized to complete the wafer processing prior to DC and RF testing as seen in Fig. 13. Due to the attachment of the relatively thick lid wafer, the thinned assembly can be processed without temporary adhesives and support substrates. A distribution metal layer followed by solder bumps completes the wafer processing; see Fig. 14. Depending on the thickness of the active device die contained

within the HIMC package cavity the final hermetic package thickness can be as thin as 0.30mm.

After completing thinning and surface mount, distribution metallization of the HMIC package wafer, final DC and RF testing can be performed utilizing industry standard, high speed, automatic wafer probing systems. Again this allows all handling associated with testing and characterization to occur at a waferscale level, as opposed to the present one-unit-at-a-time methods.

Following final test and parametric binning, singulation is accomplished by diamond saw, shown schematically in Fig. 15. At this point, the final packaged and tested components are ready for shipment either on tapeframe or in a tape and reel format.

Fig. 15. Singulated packaged die are ready for tape and reel and shipment

IV. Results

All steps of the wafer fabrication process illustrated in Fig. 4-15 have been successfully demonstrated by employing the unique capabilities of HMIC technology. The only processes that were accomplished using outside, commercially available

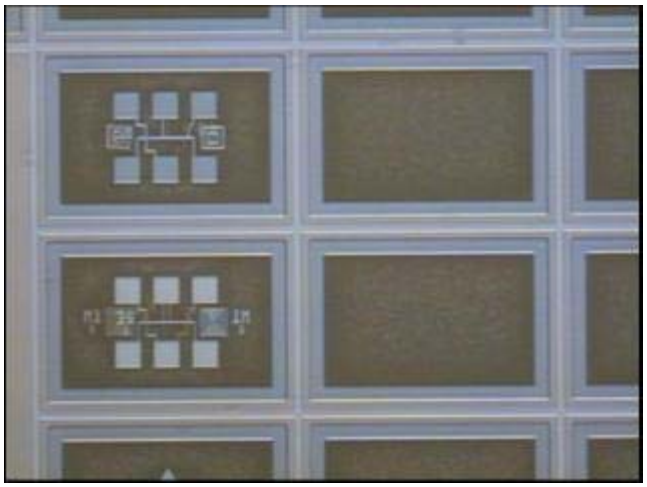

Fig. 16. Aligned and bonded lid wafer with a all glass substrate

technologies were the flip chip die tack/attach and the wafer-to-wafer bonding. .The flip chip die attach was performed using automated demonstration equipment by Datacon. The wafer to wafer alignment and subsequent bond by solder reflow was performed again by commercially available equipment by EVGroup.

To demonstrate of the aligning and bonding process capabilities of the HMIC packaging process, glass substrates with the seal ring solder metal pattern were fabricated. Fig. 16 shows the excellent alignment looking thru the clear glass substrate at the underside of the lid. The bond of the solder ring was physically tested by dicing the wafer. There was no indication of delamination or gross leaks of the 100 micron seal ring. See Fig. 17.

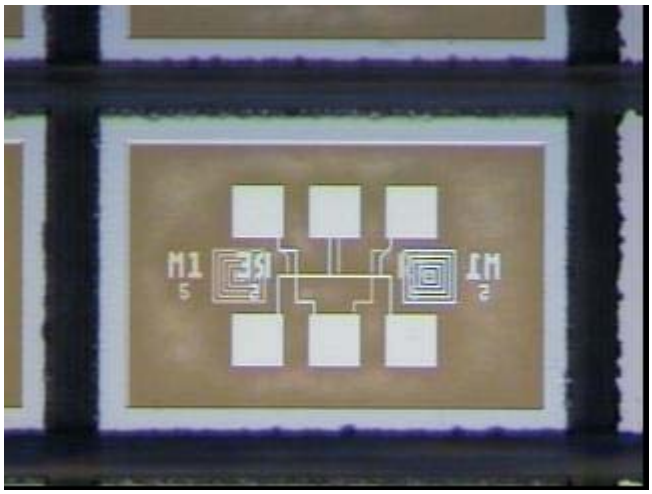

Fig. 17. Diced lid and glass bonded wafers

V. Conclusion

The HMIC package process will improve performance compared to conventional plastic or ceramic packages by reducing or eliminating wire bonds and their parasitic inductance enabling increased bandwidth and frequency response. High Q passives can be monolithically inserted with no additional wafer process steps onto the HMIC substrate reducing loss and increasing efficiency of the active devices being packaged. In addition, this HMIC packaging technology will enable designers to choose the correct junction for the function by employing mix and match materials for the active device insertion, i.e., silicon, GaAs, InP, and GaN. Lastly, the fact that all this accomplished at a waferscale level will enable high frequency components to be produced at the lowest cost. This waferscale packaging concept is analogous to the technology leap that occurred in the 1950's with the invention of the first integrated circuit for active devices. The development of this HMIC packaging concept has brought a similar scaling philosophy to the packaging arena.

Acknowledgement

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