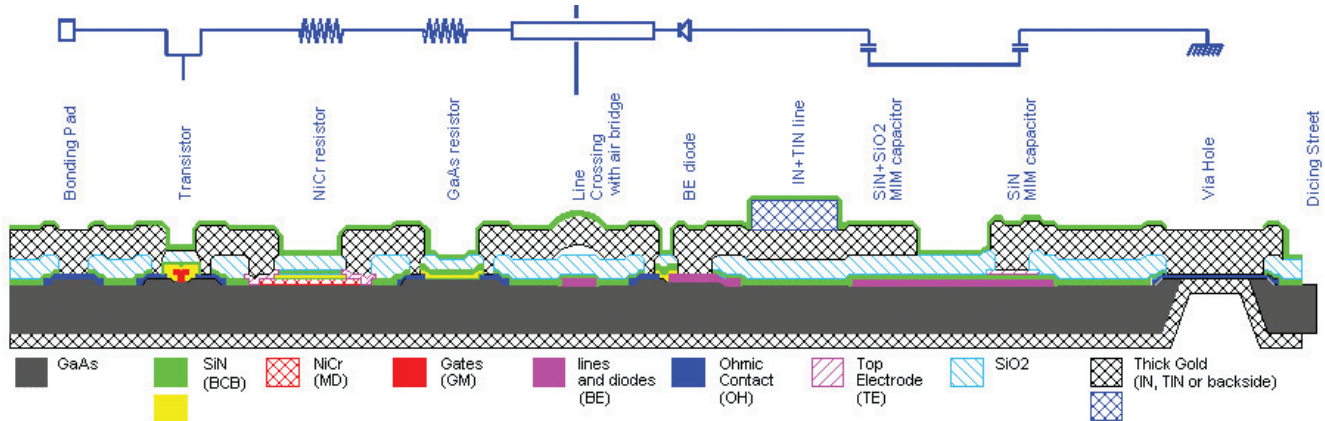


# D007IH: Fabrication Technology



D007IH process cross section

The D007IH process is based on a high Indium content epitaxial active layer, grown on a metamorphic buffer layer creating a smooth transition with the GaAs substrate. This process shows very high cut off frequency and extremely low noise and is perfectly suitable for low noise amplifiers or multifunction chips up to W band. The Technology Readiness Level (TRL from ISO-16290:2013 or ECSS-E-AS-11C) of this process is 5. After a successful space pre-evaluation completed in December 2015, the complete space evaluation of this process has been completed through an ESA\_ESTEC contract and the introduction in the ESA European Preferred Part List for space applications is in progress.

**D:** Depletion mode transistor

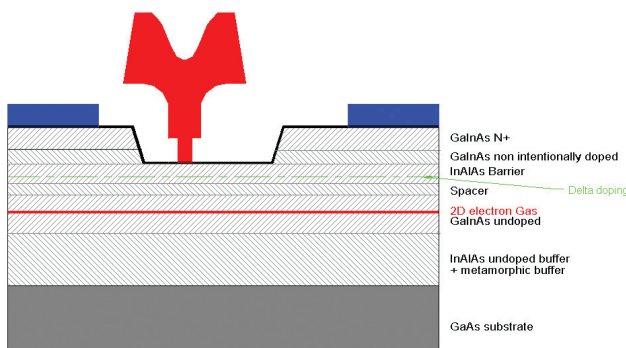
**007:** 0.07  $\mu\text{m}$  gate length

**IH:** InP like Hemt layer

## ACTIVE LAYER

The active components are based on a GaInAs-InAlAs-GaInAs-InAlAs heterostructure containing 52% of Indium and 70% of Indium in the conductive channel.

A special type of graded buffer (Metamorphic) is used to ensure a good transition between the GaAs substrate and the active layer, which are not lattice matched due to the high Indium Content.



## FEATURES

- GaInAs-InAlAs-GaInAs-InAlAs epitaxy with 52%/70% Indium content on a metamorphic buffer over a GaAs substrate
- Depletion mode recessed transistors
- 70 nm T-gates
- Two types of diodes (70 nm “GM” and 3  $\mu\text{m}$  “BE”) for mixing, level shifting, or varactors
- GaAs resistors using the active layer, non etched
- Metal resistors, using a thin film metal layer (NiCr)
- Full  $\text{Si}_3\text{N}_4$  protection ensuring high reliability
- BCB isolation around the gate to ensure low parasitic capacitances
- Two types of MIM capacitors, using the  $\text{Si}_3\text{N}_4$  layer and the  $\text{Si}_3\text{N}_4 + \text{SiO}_2$  layer
- $\text{SiO}_2/\text{Si}_3\text{N}_4 + \text{air bridge}$  isolation between layers to reduce the parasitic capacitances
- High yield 1.25  $\mu\text{m}$  thick gold metallisation for interconnections and spiral inductors. Possibility of 2.5  $\mu\text{m}$  thick lines to reduce series resistances or allow more DC current
- VIA holes through the 100  $\mu\text{m}$  or 70  $\mu\text{m}$  substrate to reduce parasitic inductances to ground

## D007IH: Fabrication Technology (continued)

### KEY PROCESS PARAMETERS

Parameter	Description	Value
Ft	Frequency Cutoff	300 GHz
MSG30	Maximum Stable Gain @ 30 GHz	17 dB
Gm	Transconductance	1.2 S/mm
Idss	Drain Source Current (Vgs = +0 V)	3000 mA/mm
Vt	Threshold Voltage	-0.5 V
NF	Minimum Noise Figure	0.5 dB @ 40 GHz
Pout	RF Power Density	100 mW/mm
CMIM_SiN	SiN MIM Capacitors	400 pF/mm <sup>2</sup>
CMIM_SiO <sub>2</sub>	SiO <sub>2</sub> MIM Capacitors	50 pF/mm <sup>2</sup>
RKN	Semiconductor Resistor Sheet Resistance	50 Ω <sup>2</sup>
RKMD	Metal Resistor Sheet Resistance	40 Ω <sup>2</sup>