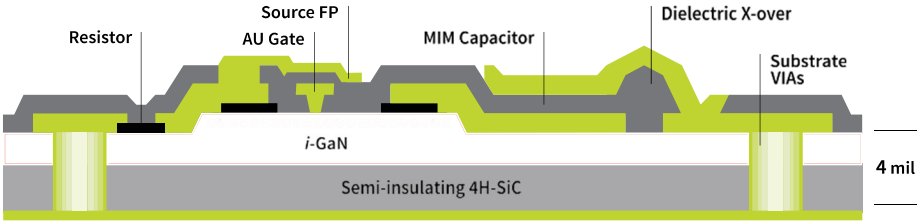
G50V3: GaN-on-SiC 0.4 µm MMIC Foundry Process

Enabling 50 V RF Designs through C-Band



PROCESS DESCRIPTION

The G50V3 is a high performance 50 V microwave process targeting applications operating at frequencies from DC through 6 GHz. The process has been fully qualified with the qualification report available upon request. The drain voltage of 50 V with breakdown of 150 V optimizes this process for high performance applications where high power and efficiency over wide bandwidths is required. The process features two gold RF interconnect layers, MMIC capacitors, thin film and bulk GaN resistors, and dielectrically supported bridges for connections to circuit elements such as capacitors and inductors. The SiC substrate thickness is 100 microns and has the smallest substrate VIA sizes available in a GaN-on-SiC MMIC process, which enables very compact FET footprint for high frequency applications. Process Design Kits (PDKs) with scalable, accurate models of the G50V3 devices are available for Microwave Office (MWO) or Advanced Design System (ADS) simulators. The PDKs have been vetted for both small signal and large signal accuracy. Model validation reports are available upon request.

The G50V3 process is offered through the foundry services using either dedicated or shared wafer runs.

FEATURES

- 0.4 µm Gate Length
- VP ~ -3 V
- 50 V Bias with >150 V Breakdown
- Performance DC – 6 GHz
- 18.3 dB Gain @ 3.5 GHz
- 10 W/mm @ 3.5 GHz
- PAE >62% @ 3.5 GHz
- Metal1 = 3 µm; Metal2 = 3 µm
- MIM Cap 180 pF/mm^2
- TFR 12 Ω/sq
- GaN Resistors: 70 and 415 Ω/sq
- Substrate Thickness: 100 µm
- Substrate VIAs
- Au Back Metal

APPLICATIONS

- SatCom
- Radar
- Telecom
- Point-to-Point Radio
- Ultra-wideband EW
- ECM

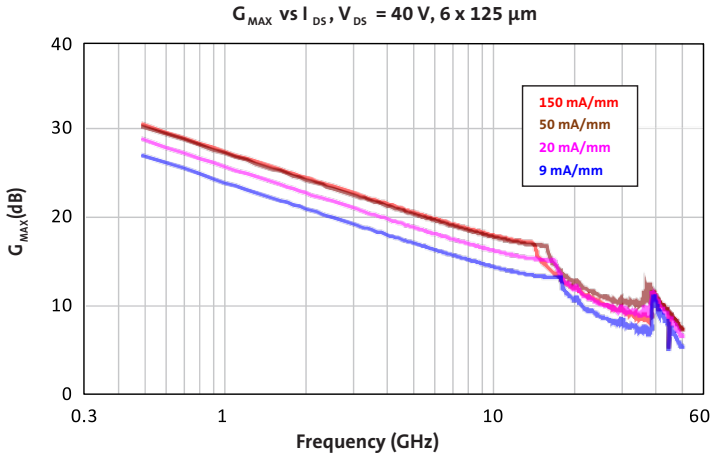
CIRCUIT TYPES

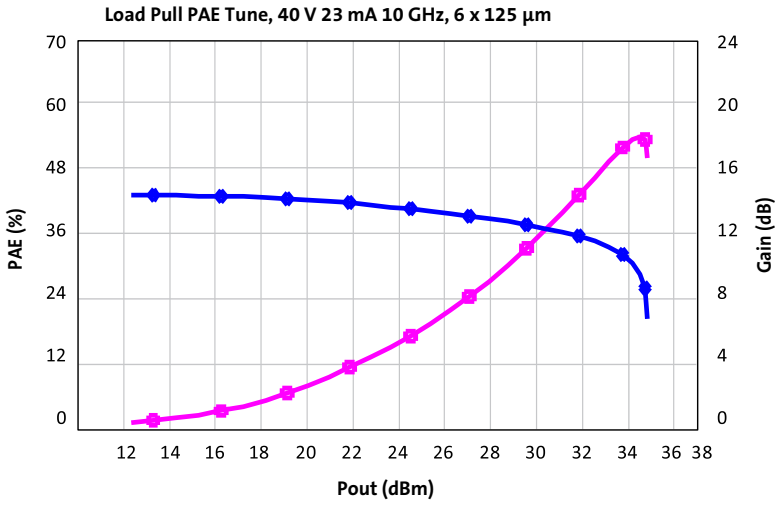
- High Power Amplifiers
- Low Noise Amplifiers
- RF Switches
- Phase Shifters
- Attenuators

G40V4: GaN-on-SiC 0.25 µm MMIC Foundry Process (continued)

FOUNDRY SERVICES

Customers can design and fabricate circuits through the foundry using either a dedicated or shared mask option. The dedicated mask provides the greatest flexibility and die count since the dedicated foundry run is completely composed of customer content. Shared masks are run quarterly. With this option, multiple customers share a single run with each customer purchasing a portion of the mask reticle into which their circuits must fit. In all cases, extreme care is taken to protect customer IP on shared masks or dedicated masks and information is always protected. Whether shared mask or dedication mask options are chosen for development, designs are easily ported to production mask sets for volume production. The foundry is a high volume manufacturer and can handle a variety of production needs.





DESIGN TOOLS

- Design Manual
- Device Library of Circuit Elements: FETs, Thin Film Resistors, Bulk Resistors, Capacitors, Inductors
- Design Kit for ADS Design Environment
- Design Kit for AWR Microwave Office
- Design Rule Check
- Thermal Reference Designs

SUPPORT FEATURES

- Process Design Kits
- Design Rule Check
- Tiling of GDSII Stream Files
- On-wafer Test Development
- Failure Analysis
- Mask Procurement
- Production 100 mm wafer
- Wafer Thinning
- Wafer Singulation
- Substrate VIAs
- DC Test
- RF On-wafer Test
- Custom Design Services
- Die Pick
- Wafer Delivery on UV Tape