

Preliminary - Rev. V2P

Features

Ka-band Power Amplifier

Gain: 25 dB

Output Power: 11.5 WSupply Voltage: 22 V

PAE: 27%Bare Die

Die Size: 3.575 x 3.075 x 0.1 mm

Applications

VSAT

1

• Ka-band Satellite Communications

Description

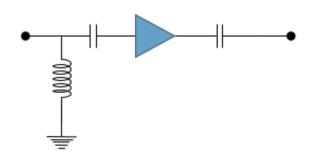
The MAPC-MP0003-DIE is a 11.5 W, Ka-band power amplifier. This GaN on SiC power amplifier operates at 22 V and has a typical power added efficiency of 27%. Typical applications include Ka-band satellite communications.

Each device is 100% RF tested to ensure performance compliance.

Ordering Information

Part Number	Package
MAPC-MP0003-DIEPPR	Bulk
MAPC-MP0003-SB1PPR	Sample Board

Functional Schematic



Pin Configuration¹

Pin #	Label
1	RF _{IN}
2, 7, 11, 12, 14, 15, 19, 24, 25	GND
3, 23	VG1, VG2
4, 22	VG3
5, 21	VG4
6, 20	VD1
8, 18	VD2
9, 17	VD3
10, 16	VD4
13	RF _{OUT}

The backside of the die must be connected to RF, DC and thermal ground.

^{*} Restrictions on Hazardous Substances, compliant to current RoHS EU directive.



Pin Description

Pin #	Name	Description
1	RF _{IN}	RF Input has DC ground for ESD robustness
2, 7, 11, 12, 14, 15, 19, 24, 25	GND	RF and DC Ground
3, 23	VG1, VG2	Gate voltage, stages 1 and 2
4, 22	VG3	Gate voltage, stage 3
5, 21	VG4	Gate voltage, stage 4
6, 20	VD1	Drain voltage, stage 1
8, 18	VD2	Drain voltage, stage 2
9, 17	VD3	Drain voltage, stage 3
10, 16	VD4	Drain voltage, stage 4
13	RF _{OUT}	RF Output is DC de-coupled



Preliminary - Rev. V2P

Electrical Specifications:

Freq. = 27 - 31 GHz, T_C = 25°C, V_D = +22 V, I_{DQ} = 300 mA, CW Operation, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Тур.	Max.
Gain	Small Signal, P_{IN} = -10 dBm Large Signal, P_{IN} = +21 dBm	dB		25.0 19.6	_
Gain Flatness (Peak-to-Peak)	P _{IN} = -10 dBm	dB	_	2	
IM3	P _{OUT} = 33 dBm per tone, spacing 100 kHz to 1 GHz	dBc	_	25	_
Output Power	P _{IN} = +21 dBm	dBm		40.6	
Output Power Flatness	P _{IN} = +21 dBm	dB		1	
Input Return Loss	P _{IN} = -10 dBm	dB	_	12	_
Output Return Loss	P _{IN} = -10 dBm	dB	_	10	_
Power Added Efficiency P _{IN} = +21 dBm		%	_	27	_

Recommended Operating Conditions

Parameter	Symbol	Unit	Min.	Тур.	Max.
RF Input Power	RF _{IN}	dBm	_	21	25
Drain Supply Voltage	VD	V	_	22	25
Gate Supply Voltage	VG	V	-5	-3.9	_
CW Duty Cycle		%	10	_	100
Junction Temperature ^{4,5}	TJ	°C	_	+200	_
Operating Temperature ⁶	T _C	°C	-40	_	+85
Storage Temperature	Ts	°C	-55	_	150

Absolute Maximum Ratings^{5,6}

Parameter	Symbol	Unit	Min	Max
RF Input Power	RF _{IN}	dBm	_	28
Drain Supply Voltage	VD	V		28
Gate Supply Voltage	VG	V	-6	_
Junction Temperature	TJ	°C	_	+225
Storage Temperature	Ts	°C	-55	+150

- 2. Exceeding any one or combination of these limits may cause permanent damage to this device.
- 3. MACOM does not recommend sustained operation near these survivability limits.
- 4. Operating at nominal conditions with $T_J \le +200$ °C will ensure MTTF > 1 x 10⁶ hours.
- 5. Junction Temperature $(T_J) = T_C + \Theta jc * (V * I-(P_{OUT}-P_{IN}))$

Typical thermal resistance (Θ jc) = 3.2 °C/W.

a) For T_C = +25°C, Pout = 40.6 dBm, Pin = 21 dBm:

T_{.J} = 129 °C @ 22 V, 2.0 A

b) For T_C = +85°C, Pout = 39.5 dBm, Pin = 21 dBm:

T_J = 184 °C @ 22 V, 1.7 A

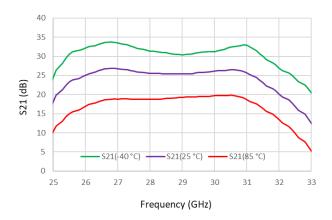
6. T_C is defined as backside of die

PRELIMINARY: Data Sheets contain information regarding a product MACOM has under development. Performance is based on engineering tests. Specifications are typical. Mechanical outline has been fixed. Engineering samples and/or test data may be available. Commitment to produce in volume is not guaranteed.

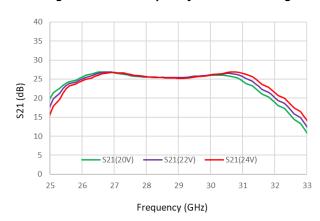


Typical Performance Curves: V_D = 22 V, I_{DSQ} = 300 mA, V_G = -3.9 V typical

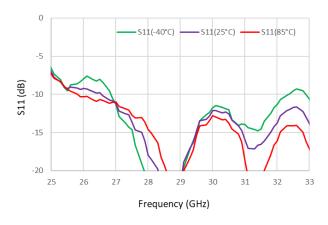
Small Signal Gain vs. Frequency over Temperature



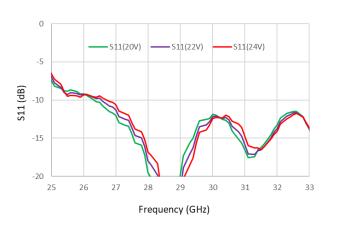
Small Signal Gain vs. Frequency over Bias Voltage



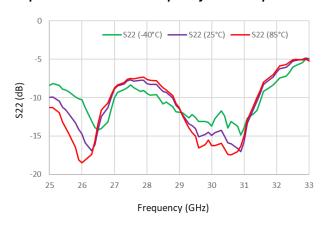
Input Return Loss vs. Frequency over Temperature



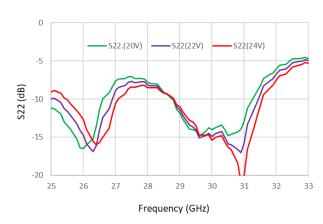
Input Return Loss vs. Frequency over Bias Voltage



Output Return Loss vs. Frequency over Temperature



Output Return Loss vs. Frequency over Bias Voltage



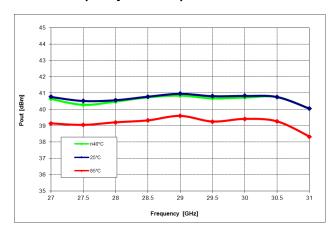
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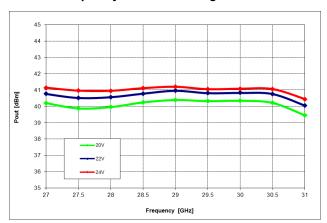


Typical Performance Curves: $V_D = 22 \text{ V}$, $I_{DSQ} = 300 \text{ mA}$, $V_G = -3.9 \text{ V}$ typical, Pin = 21 dBm

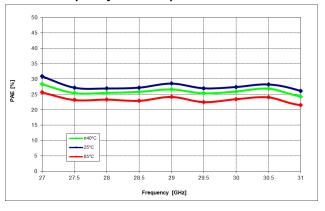
Pout vs. Frequency over Temperature



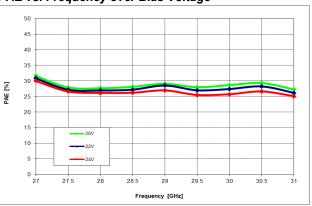
Pout vs. Frequency over Bias Voltage



PAE vs. Frequency over Temperature

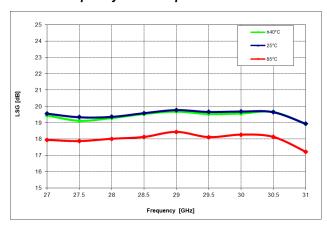


PAE vs. Frequency over Bias Voltage

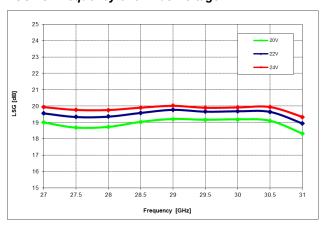


LSG vs. Frequency over Temperature

5



LSG vs. Frequency over Bias Voltage



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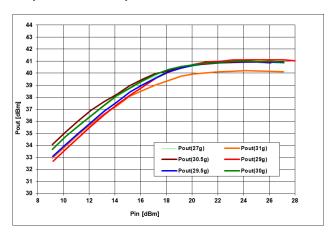
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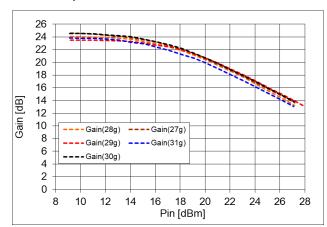
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Typical Performance Curves: $V_D = 22 \text{ V}$, $I_{DSQ} = 300 \text{ mA}$, $V_G = -3.9 \text{ V}$ typical, 25°C

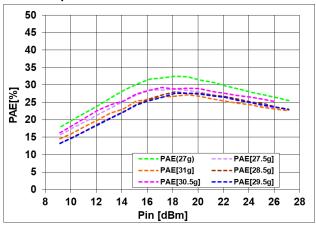
Output Power vs. Input Power at 25°C



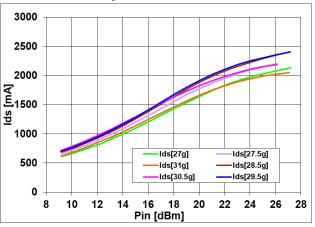
Gain vs. Input Power at 25°C



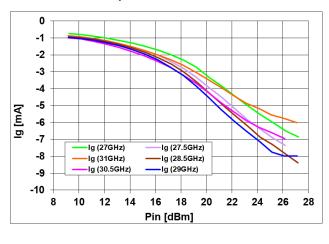
PAE vs. Input Power at 25°C



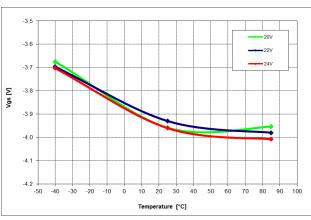
Drain Current vs. Input Power at 25°C



Gate Current vs. Input Power at 25°C



Gate Voltage vs. Temperature for constant Idsq



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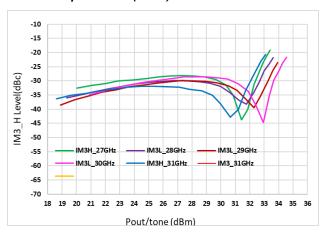
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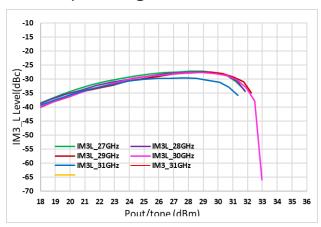
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Typical Performance Curves: $V_D = 22 \text{ V}$, $I_{DSQ} = 300 \text{ mA}$, $V_G = -3.9 \text{ V}$ typical

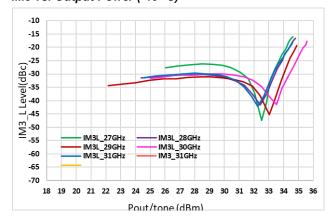
IM3 vs. Output Power (25 °C)



IM3 vs. Output Power @ 85°C



IM3 vs. Output Power (-40 °C)

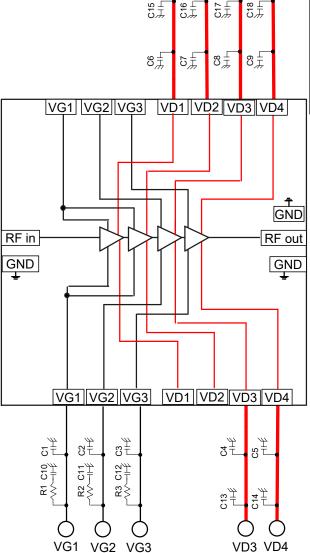




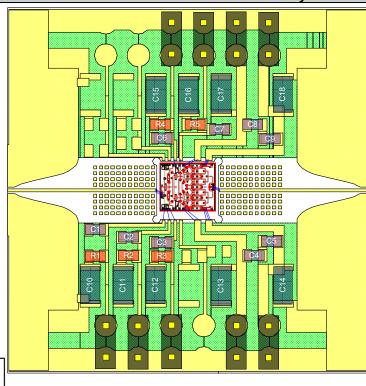
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Sample Board Layout

Application Schematic



VD1 VD2 VD3 VD4



Parts List

Part	Value	Case Style
C1 – C9	0.01 μF, 50 V	1206
C10- C18	10 μF, 50 V	0603
R1 – R3	10 Ω	0402

Sample Board Material Specifications

Top Layer: 1/2 oz Copper Cladding, 0.017 mm thickness Dielectric Layer: Rogers RO4350B 0.101 mm thickness Bottom Layer: 1/2 oz Copper Cladding, 0.017 mm thickness Finished overall thickness: 0.135 mm

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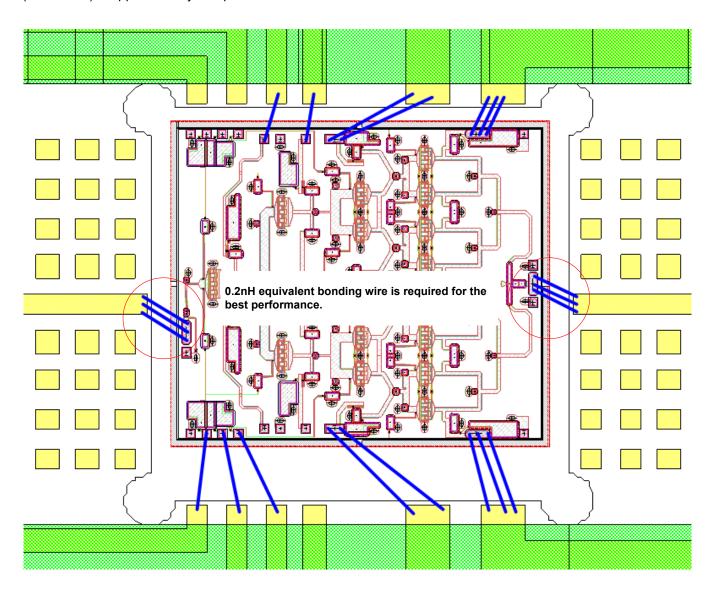
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8



Recommended Bonding Diagram and PCB Layout Detail:

Optimum bonding wire inductance for the RF I/O connection is 0.2 nH, and physical length for the gold bond wire (0.001" dia.) is approximately 350 µm each for the three wire connection.





Preliminary - Rev. V2P

Application Notes

MAPC-MP0003-DIE is designed to be easy to use yet high performance. The ultra small size and simple bias allows easy placement on system board. RF output ports are DC de-coupled internally. RF input port has DC connection to the ground for the ESD protection purpose.

Die Attachment

This product is manufactured from 0.1 mm (0.004") thick SiC substrate and has vias through to the backside to enable grounding to the circuit.

Recommended conductive epoxy is Namics Unimec XH9890-6. Epoxy should be applied and cured in accordance with the manufacturer's specifications and should avoid contact with the top of the die.

Supply Sequencing Turn-on

- 1. Apply V_G (-5 V).
- 2. Apply V_D (22 V typical).
- 3. Set I_{DQ} by adjusting V_G more positive (typically V_{G^*} -3.9 V for I_{DQ} = 300 mA).
- 4. Apply RF_{IN} signal.

Turn-off

- 1. Remove RF_{IN} signal.
- 2. Decrease V_G to -5 V.
- 3. Decrease V_D to 0 V.

Biasing Conditions

Recommended biasing conditions are: $V_D = 22 \text{ V}$, $I_{DQ} = 300 \text{ mA}$ (controlled with V_G).

 V_{D} bias must be applied to $V_{\text{D}}1,\ V_{\text{D}}2,\ V_{\text{D}}3,$ and $V_{\text{D}}4$ pads.

Both V_D3 pads (9, 17) are required for current symmetry.

Both V_D4 pads (10, 16) are required for current symmetry.

A single DC voltage (V_G) will bias all amplifier stages. Muting can be accomplished by setting the V_G to the pinched off voltage (V_G = -5 V).

Handling Procedures

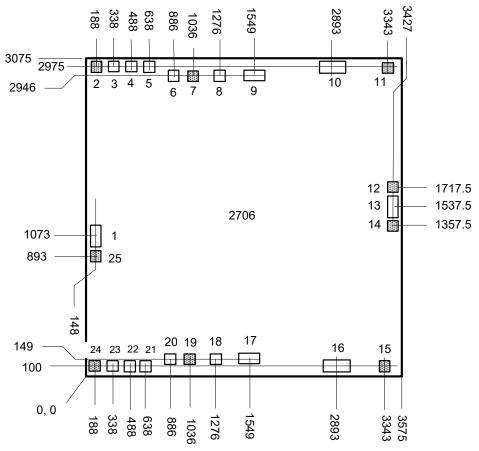
Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.



Die Dimensions



Die thickness is 100 +/- 10 μm .

Revision history

Rev	Date	Change description
V1P	1/30/23	Preliminary data sheet release
V2P	6/6/23	Update outline, pinout, and sample board to reflect three gate pins.



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