Features

- Ka-Band Power Amplifier
- Gain: 25 dB
- Output Power: 6 W
- Supply Voltage: 22 V
- PAE: 27%
- Bare Die
- Die Size: 3.575 x 1.75 x 0.1 mm

Applications

- Ka-band Satellite Communications

Description

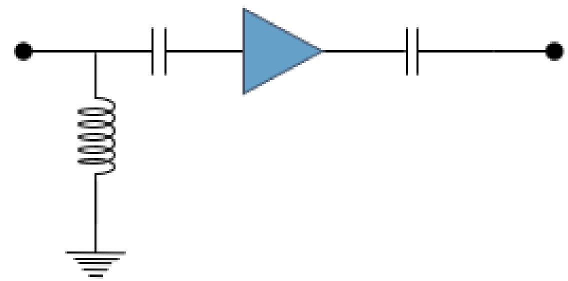
The MAPC-MP0013-DIE is a 6 W, Ka-band power amplifier. This GaN on SiC power amplifier operates at 22 V and has a typical power added efficiency of 27%. Typical applications include Ka-band satellite communications.

Each device is 100% RF tested to ensure performance compliance.

Ordering Information

Part Number	Package
MAPC-MP0013-DIEPPR	Bulk
MAPC-MP0013-SB1PPR	Sample Board

Functional Schematic



Pin Configuration[1]

Pin #	Label
1	RF_{IN}
2, 7, 11, 12, 14, 15, 19, 24, 25	GND
3, 23	VG1, VG2
4, 22	VG3
5, 21	VG4
6, 20	VD1
8, 18	VD2
9, 17	VD3
10, 16	VD4
13	RF_{OUT}

1. The backside of the die must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Pin Description

Pin #	Name	Description
1	RF_{IN}	RF Input has DC ground for ESD robustness
2, 7, 11, 12, 14, 15, 19, 24, 25	GND	RF and DC Ground
3, 23	VG1, VG2	Gate voltage, stages 1 and 2
4, 22	VG3	Gate voltage, stage 3
5, 21	VG4	Gate voltage, stage 4
6, 20	VD1	Drain voltage, stage 1
8, 18	VD2	Drain voltage, stage 2
9, 17	VD3	Drain voltage, stage 3
10, 16	VD4	Drain voltage, stage 4
13	RF_{OUT}	RF Output is DC de-coupled

Electrical Specifications:
Freq. = 27 - 31 GHz, T_C = 25°C, V_D = +22 V, I_{DQ} = 150 mA, CW Operation, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	Small Signal, P_{IN} = -10 dBm Large Signal, P_{IN} = +21 dBm	dB	—	25 17	—
Gain Flatness (Peak-to-Peak)	P_{IN} = -10 dBm	dB	—	1	—
IM3	P_{OUT} = 31 dBm per tone, spacing 100 kHz to 1 GHz	dBc	—	25	—
Output Power	P_{IN} = +21 dBm	dBm	—	38	—
Output Power Flatness	P_{IN} = +21 dBm	dB	—	2	—
Input Return Loss	P_{IN} = -10 dBm	dB	—	8	—
Output Return Loss	P_{IN} = -10 dBm	dB	—	10	—
Power Added Efficiency	P_{IN} = +21 dBm	%	—	27	—

Recommended Operating Conditions

Parameter	Symbol	Unit	Min.	Typ.	Max.
RF Input Power	RF_{IN}	dBm	—	21	25
Drain Supply Voltage	VD	V	—	22	25
Gate Supply Voltage	VG	V	-5	—	—
Duty Cycle		%	—	10	100
Junction Temperature[4,5]	T_j	°C	—	—	200
Operating Temperature[6]	T_c	°C	-40	—	+85
Storage Temperature	T_s	°C	-55	—	+150

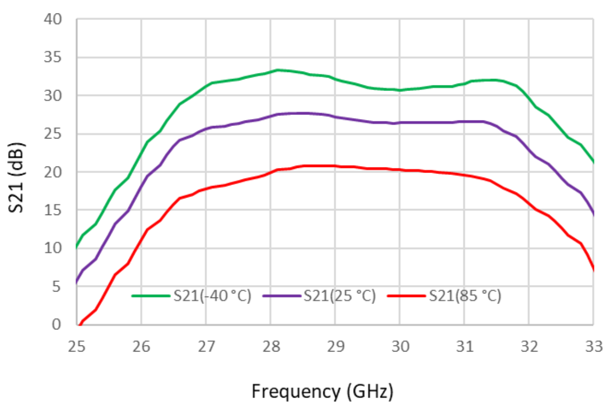
Absolute Maximum Ratings[5,6]

Parameter	Symbol	Unit	Min	Max
RF Input Power	RF_{IN}	dBm	—	28
Drain Supply Voltage	VD	V	—	28
Gate Supply Voltage	VG	V	-6	—
Junction Temperature	T_J	°C	—	+225
Storage Temperature	T_S	°C	-55	+150

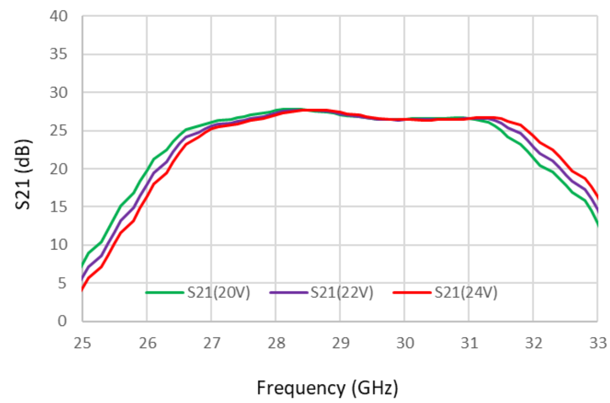
2. Exceeding any one or combination of these limits may cause permanent damage to this device.
3. MACOM does not recommend sustained operation near these survivability limits.
4. Operating at nominal conditions with $T_J \leq$ +200 °C will ensure MTTF > 1 x 10^6 hours.
5. Junction Temperature (T_J) = T_C + Θjc * (V * I-(P_{OUT}-P_{IN}))
   Typical thermal resistance (Θjc) = 5.2 °C/W.
a) For T_C = +25°C, Pout = 38 dBm, Pin = 21 dBm:
   T_J = 121 °C @ 22 V, 1.1 A
b) For T_C = +85°C, Pout = 37 dBm, Pin = 21 dBm:
   T_J = 174 °C @ 22 V, 1.0 A
6. T_C is defined as backside of die

Typical Performance Curves:

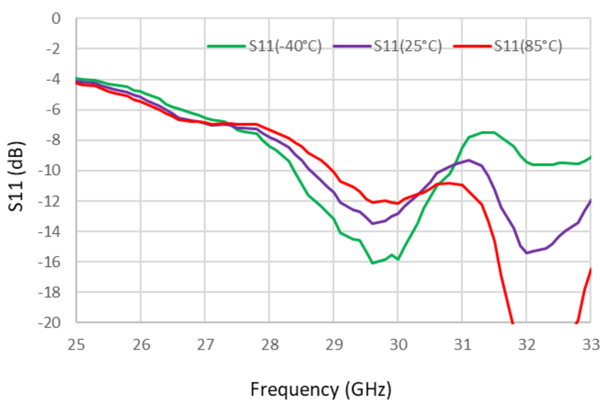
Small Signal Gain vs. Frequency over Temperature



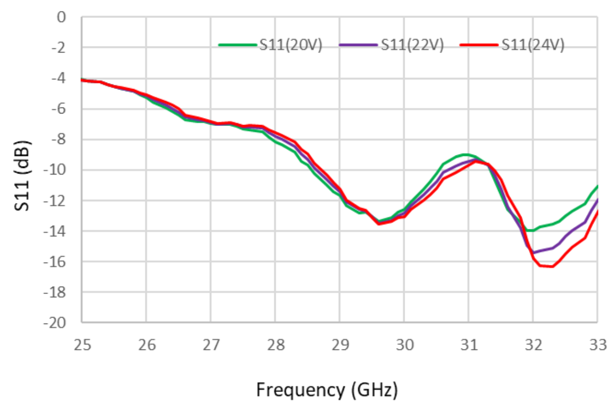
Small Signal Gain vs. Frequency over Bias Voltage



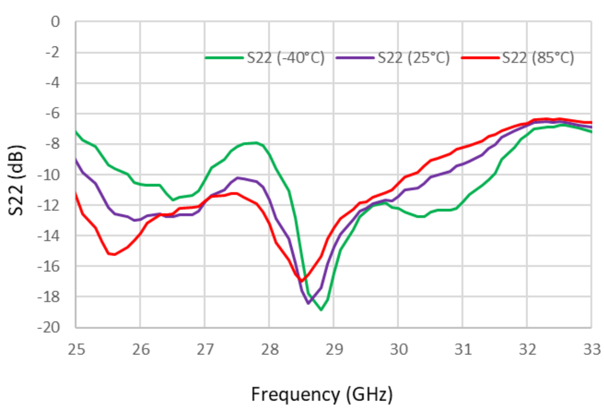
Input Return Loss vs. Frequency over Temperature



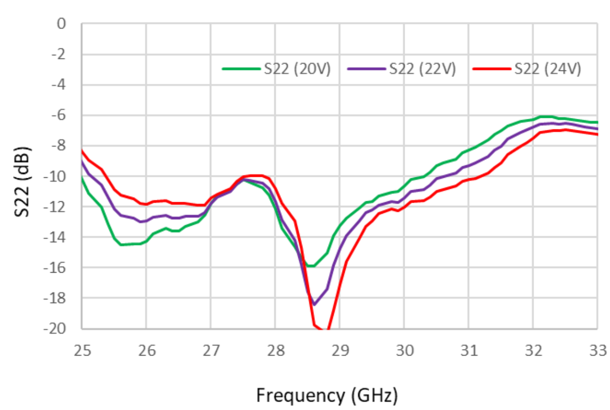
Input Return Loss vs. Frequency over Bias Voltage



Output Return Loss vs. Frequency over Temperature

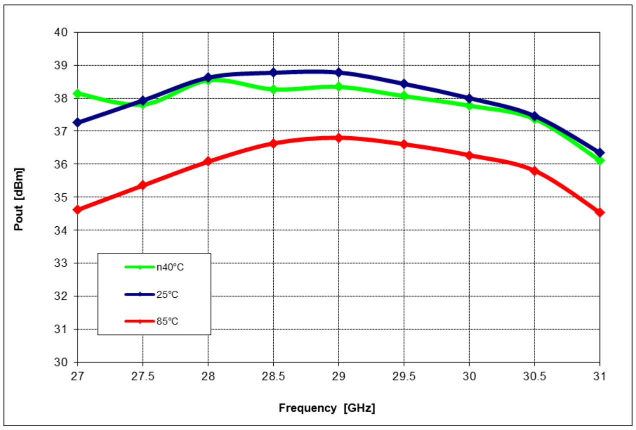


Output Return Loss vs. Frequency over Bias Voltage

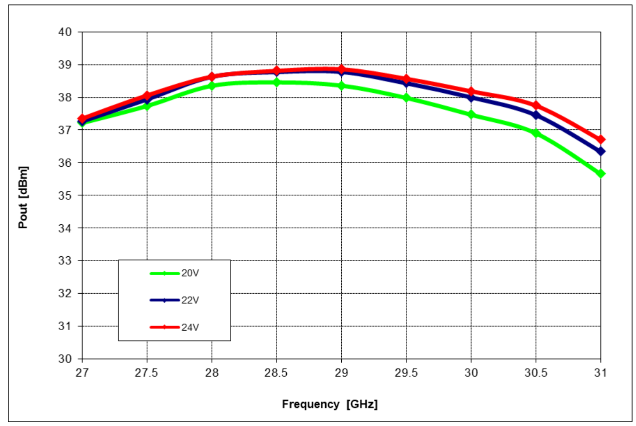


Typical Performance Curves:

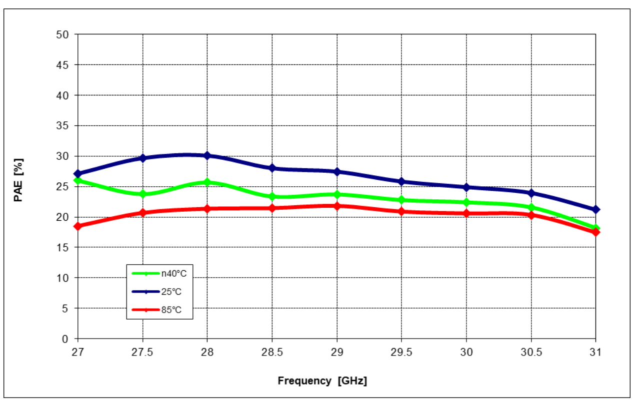
Pout vs. Frequency over Temperature



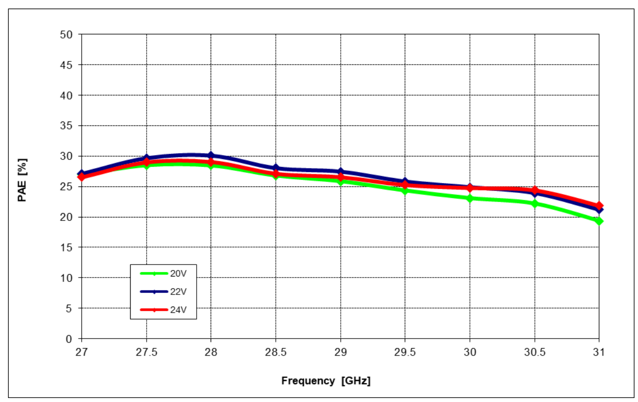
Pout vs. Frequency over Bias Voltage



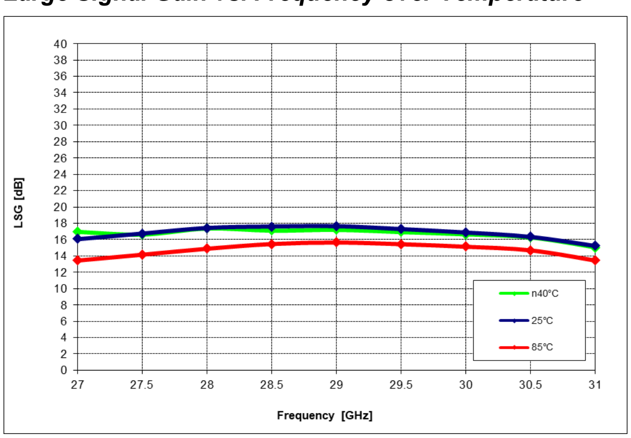
PAE vs. Frequency over Temperature



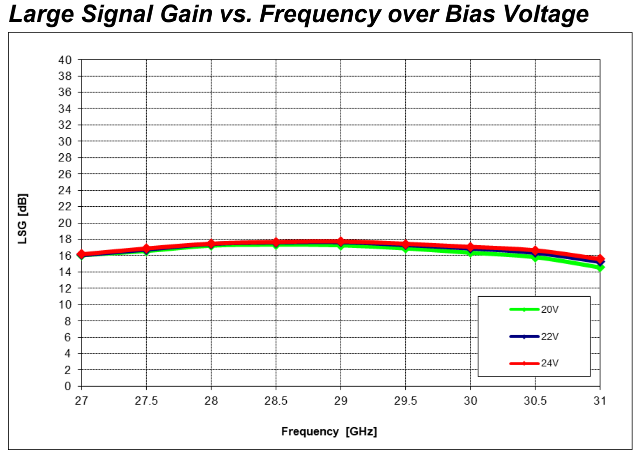
PAE vs. Frequency over Bias Voltage



Large Signal Gain vs. Frequency over Temperature

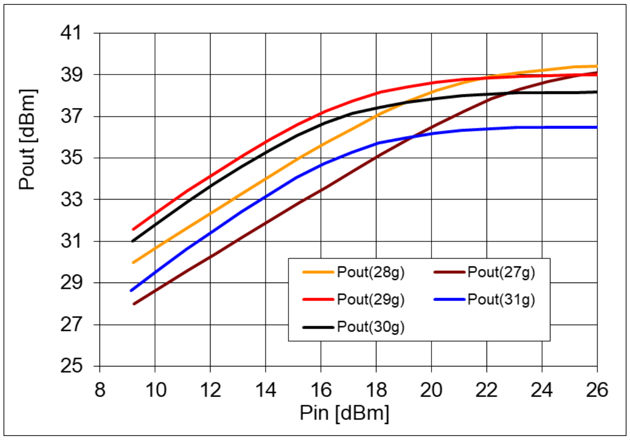


Large Signal Gain vs. Frequency over Bias Voltage

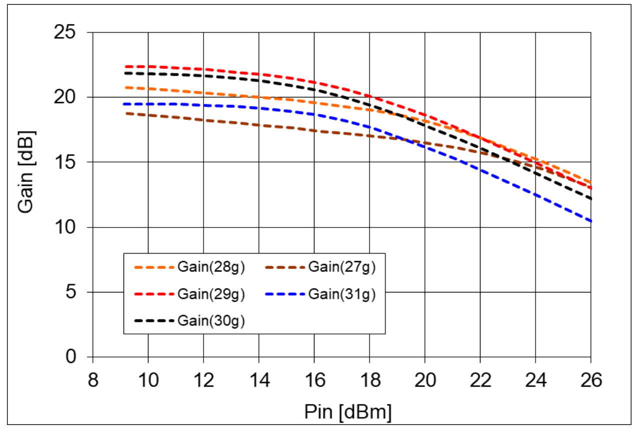


Typical Performance Curves:

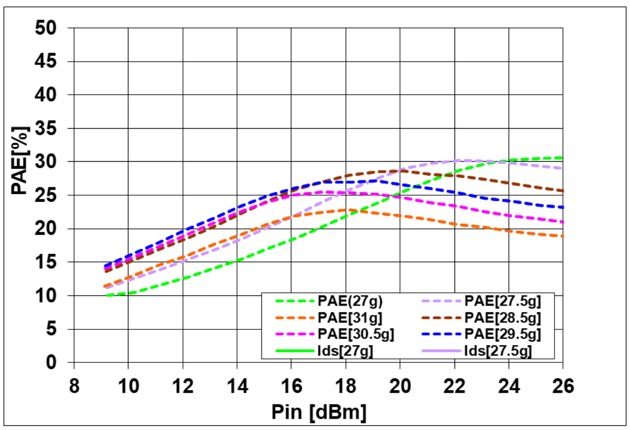
Output Power vs. Input Power at 25°C



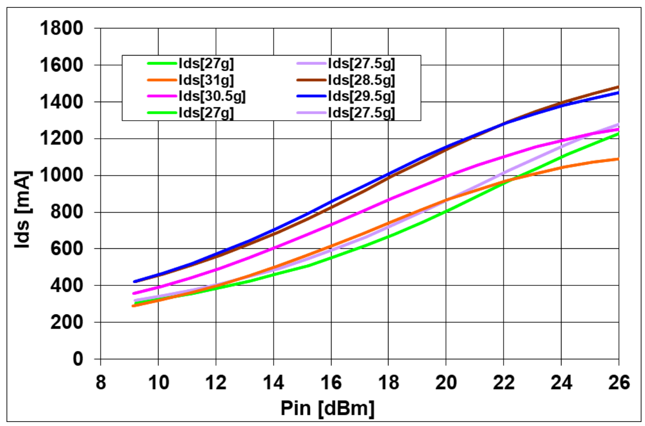
Gain vs. Input Power at 25°C



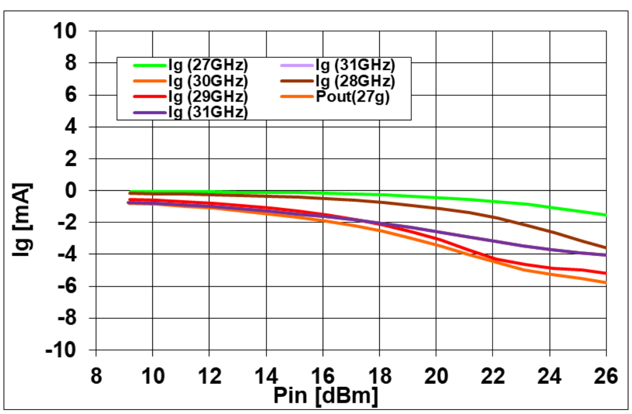
PAE vs. Input Power at 25°C



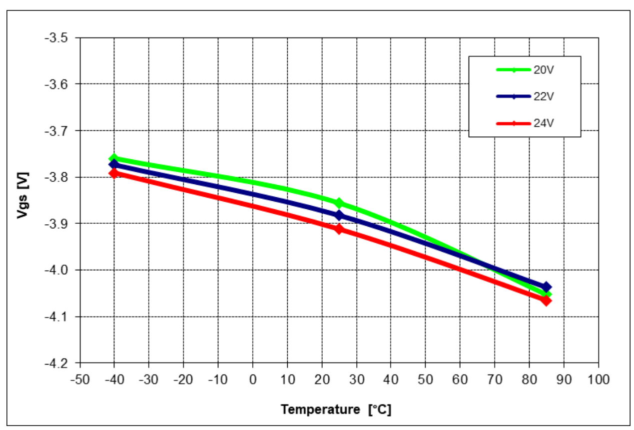
Drain Current vs. Input Power at 25°C



Gate Current vs. Input Power at 25°C

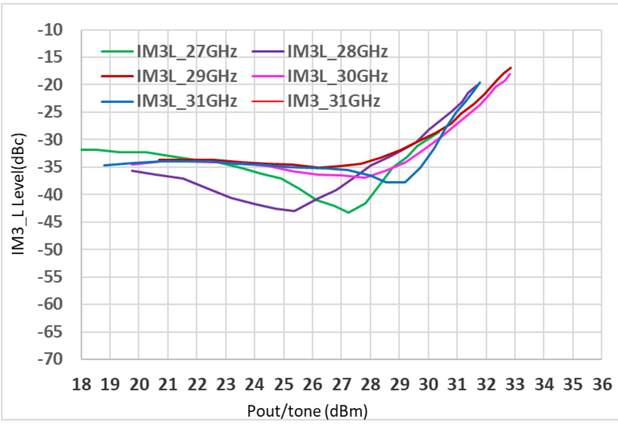


Gate Voltage vs. Temperature for Constant Idsq

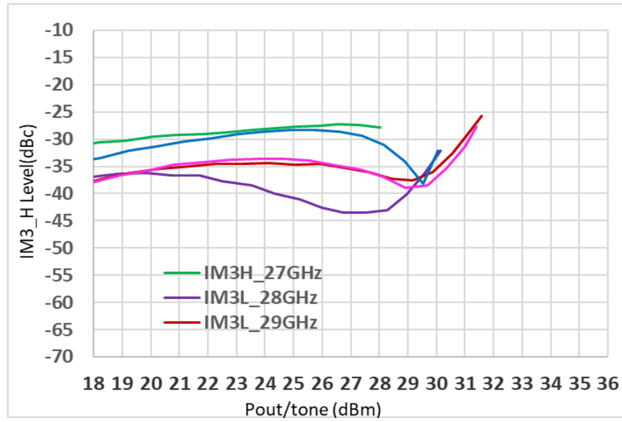


Typical Performance Curves:

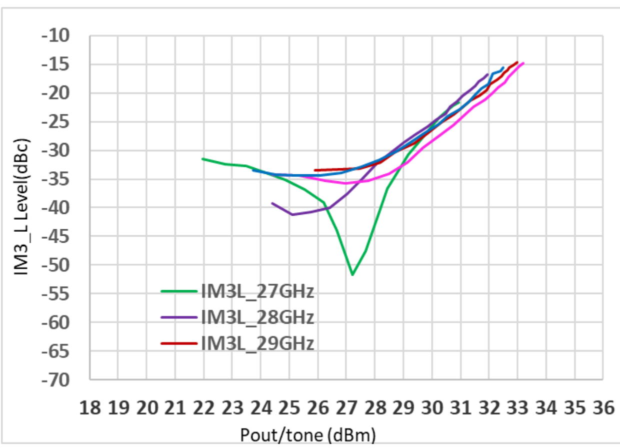
IM3 vs. Output Power (25 °C)



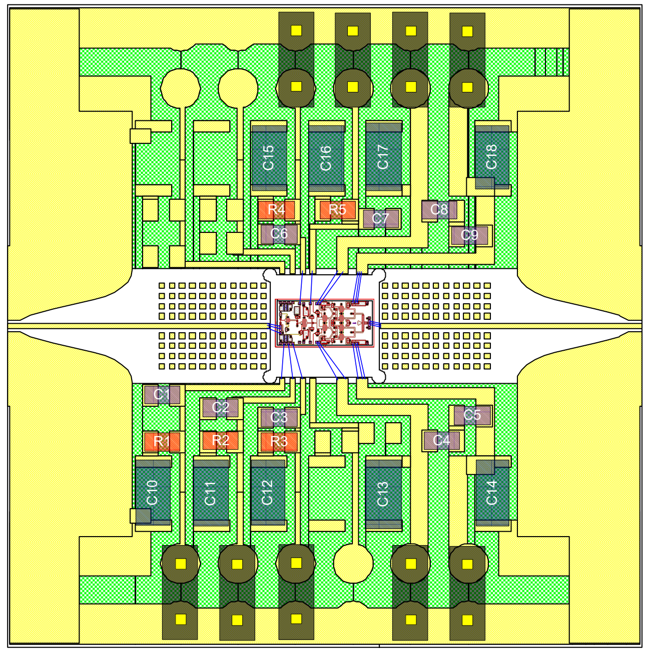
IM3 vs. Output Power @ 85˚C



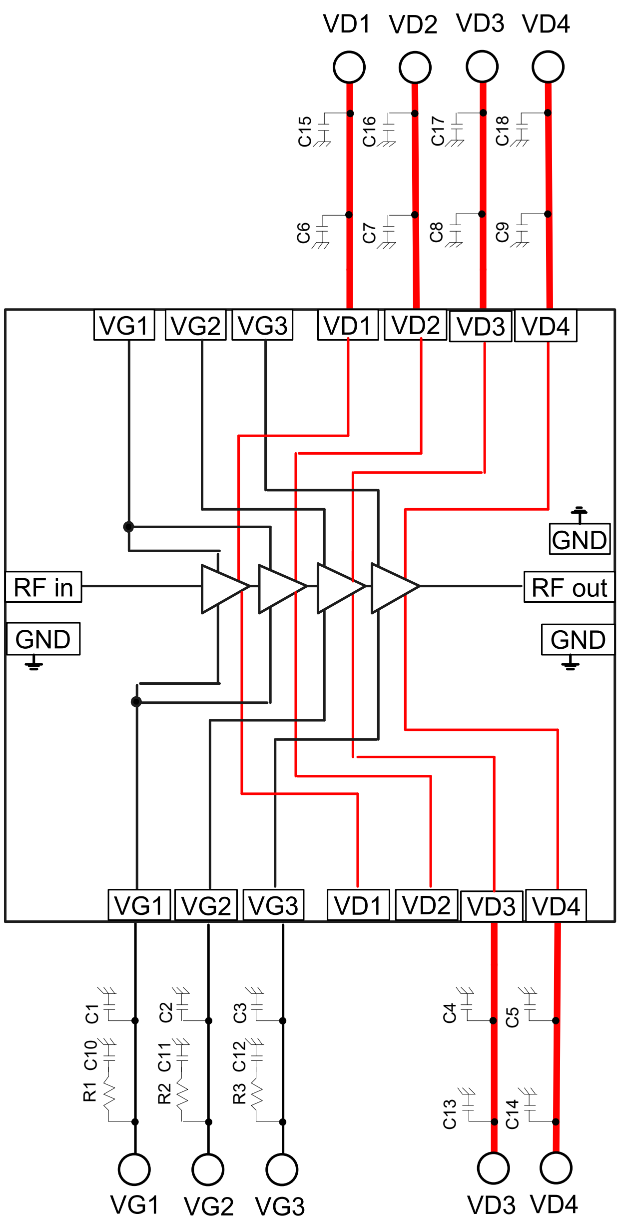
IM3 vs. Output Power (-40 °C)



Sample Board Layout



Application Schematic



Parts List

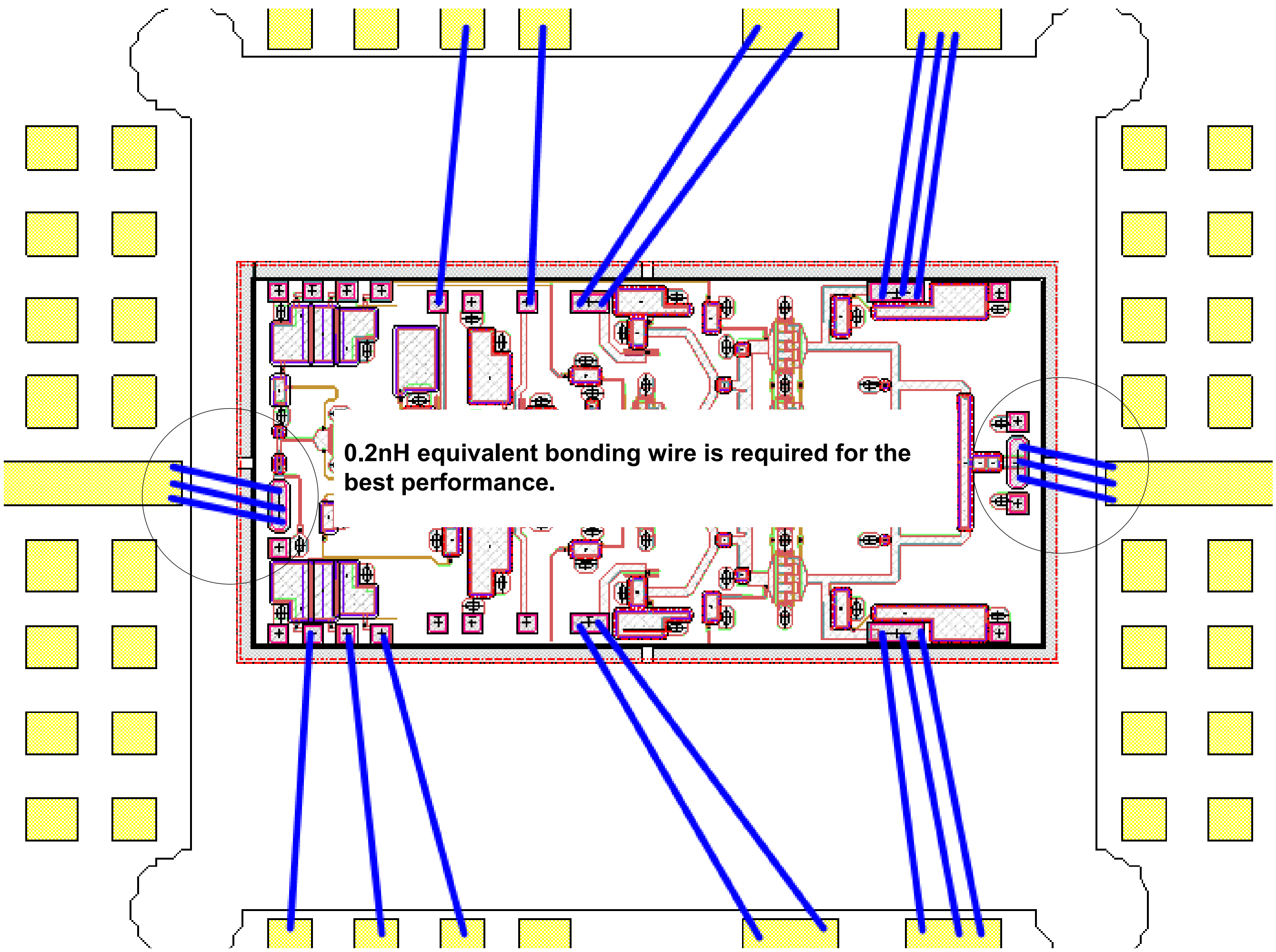
Part	Value	Case Style
C1 – C9	0.01 µF, 50V	1206
C10– C18	10 µF, 50V	0603
R1 – R3	10 Ω	0402

Sample Board Material Specifications

Top Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Dielectric Layer: Rogers RO4350B 0.101 mm thickness
Bottom Layer: 1/2 oz Copper Cladding, 0.017 mm thickness
Finished overall thickness: 0.135 mm

Recommended Bonding Diagram and PCB Layout Detail:

Optimum bonding wire inductance for the RF I/O connection is 0.2 nH, and physical length for the gold bond wire (.001” dia.) is approximately 350 µm each for the three wire connection.



Application Notes

MAPC-MP0013-DIE is designed to be easy to use yet high performance. The ultra small size and simple bias allows easy placement on system board. RF output ports are DC de-coupled internally. RF input port has DC connection to the ground for the ESD protection purpose.

Die Attachment

This product is manufactured from 0.1 mm (0.004”) thick SiC substrate and has vias through to the backside to enable grounding to the circuit.

Recommended conductive epoxy is Namics Unimec XH9890-6. Epoxy should be applied and cured in accordance with the manufacturer’s specifications and should avoid contact with the top of the die.

Supply Sequencing

Turn-on

1. Apply V_G (-5 V).
2. Apply V_D (22 V typical).
3. Set I_{DQ} by adjusting V_G more positive (typically V_G~ -3.9 V for I_{DQ} = 150 mA).
4. Apply RF_{IN} signal.

Turn-off

1. Remove RF_{IN} signal.
2. Decrease V_G to -5 V.
3. Decrease V_D to 0 V.

Biasing Conditions

Recommended biasing conditions are:
V_D = 22 V, I_{DQ} = 150 mA (controlled with V_G).

V_D bias must be applied to V_D1, V_D2, V_D3, and V_D4 pads.

Both V_D3 pads (9, 17) are required for current symmetry.

Both V_D4 pads (10, 16) are required for current symmetry.

A single DC voltage (V_G) will bias all amplifier stages. Muting can be accomplished by setting the V_G to the pinched off voltage (V_G = -5 V).

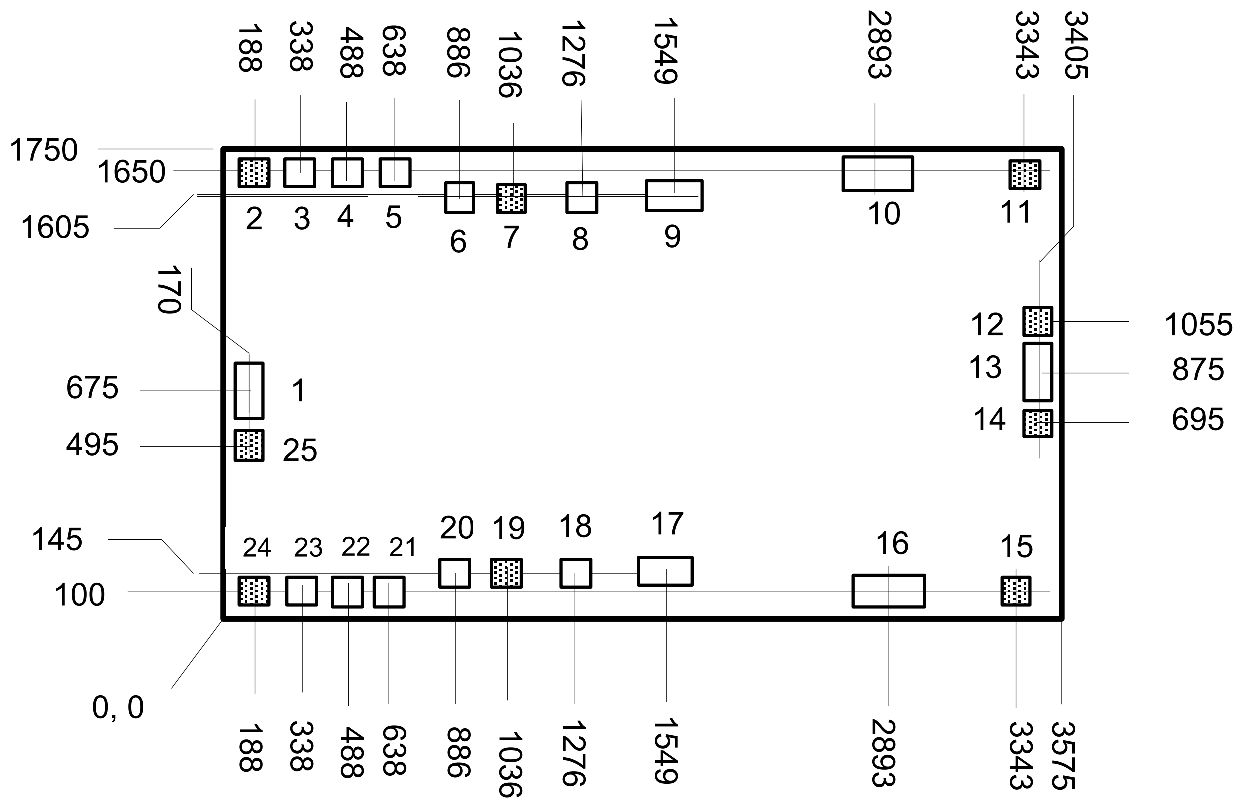
Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.

Die Dimensions



Die thickness is 100 +/- 10 µm.

Revision history

Rev	Date	Change description
V1P	1/31/23	Release of preliminary data sheet
V2P	6/6/23	Update outline, pinout, and sample board to reflect three gate pins.